UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,971	08/22/2003	Henry Samueli	50931/PAN/B600	1069

23363 7590 09/14/2004

CHRISTIE, PARKER & HALE, LLP
PO BOX 7068
PASADENA, CA 91109-7068

EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,971	SAMUELI ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030822*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-9 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Blazo U.S. patent No 5,754,437.

As per claim 1, Blazo teaches a signal processing system for converting a variable frequency input signal to a fixed frequency output signal comprising: means for generating a first clock signal (see figs. 3, 4a elements 34 and 70 and col.7, line 44 and col.8, line 63) at a first clock frequency; means for receiving a frequency control (see figs. 3, 4a element 44 and col.7, lines 66-67 and col.8, line 1-15) signal that corresponds to a second frequency; means generating a second clock signal at the second frequency as a function of said frequency control signal (see figs. 3, 4a element 46 and col.7, lines 66-col.8, line 1-15); a phase detector is the same as the claimed (means for generating a phase offset) signal representing an offset in phase between the first clock signal and the second clock signal (see figs. 3, 4a element 48 and col.8, lines 1-4 and col.9, lines 5-17 and col.10, lines 25-26); and means for converting a variable frequency input signal to an interpolated signal (see fig.4b element 76 and col.12, lines50-54 and col.18, lines 50-53) at a fixed sampling frequency in accordance with said phase offset signal.

As per claim 3, Blazo inherently teaches the means for converting a variable frequency input signal to an interpolated signal at a fixed sampling frequency in accordance with said phase offset signal comprises an interpolator that interpolates the variable frequency input signal by a non-integer value.

As per claim 4, Blazo inherently includes means for converting a variable frequency input wherein the signal an interpolated signal at a fixed sampling frequency in accordance with said phase offset signal comprises an interpolator that interpolates the variable frequency input signal by an integer value.

As per claim 5, Blazo teaches a signal processing system for converting a variable frequency input signal to an output signal having a fixed output frequency, comprising: means for generating a clock signal at a clock frequency (see figs. 3, 4a element 46 and col.7, lines 66-col.8, line 1-15) equal to baud rate of said variable frequency input signal as a function of a frequency control signal; a phase detector is the same as the claimed (means for generating a phase offset) (see figs. 3, 4a element 48 and col.8, lines 1-4 and col.9, lines 5-17 and col.10, lines 25-26) signal representing an offset in phase between a recipient clock signal (see figs.3 and 4a elements 34 and 70) and the clock signal; and means for converting a variable frequency input signal to an interpolated signal (see fig.4b element 76 and col.12, lines50-54 and col.18, lines 50-53) at a fixed sampling frequency in accordance with said phase offset signal.

As per claim 6, Blazo teaches a signal processing system, comprising: means for providing a first clock signal at a first clock frequency (see figs.3 and 4a elements 34 and 70); oscillator means (see fig. 4a element 66 and col.8, line 56 and col.9, lines 18-30), responsive to a frequency control signal and the first clock signal for providing an output clock signal at a fixed

second clock frequency and a phase detector is the same as the claimed (phase offset) (see figs. 3, 4a element 48 and col.8, lines 1-4 and col.9, lines 5-17 and col.10, lines 25-26) signal representing an offset in phase between the first clock signal and the second clock signal, and interpolation means (see fig.4b element 76 and col.12, lines50-54 and col.18, lines 50-53) for offsetting a pair of variable frequency input signals in accordance with the phase offset signal to provide an interpolated signal at a fixed output sampling frequency.

As per claim 7, Blazo inherently includes wherein offset signal is greater than or equal to zero and the phase less than one.

As per claim 8, Blazo inherently includes wherein the interpolation means interpolates the variable frequency input signal by a non-integer value.

As per claim 9, Blazo inherently includes wherein the interpolation means interpolates the variable frequency input signal by an integer value.

As per claim 12, Blazo includes said interpolation means includes a register (see fig.4a element 64 and col.9, lines 55-56) responsive said second clock signal, to provide said pair variable frequency input signals.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blazo U.S. Patent No 5,754,437 in view of Cova U.S. patent No 6,141,390.

As per claims 2 and 10, Blazo teaches all the features and analog converter (see fig.4b element 84) of the claimed invention except means for modulating the interpolated signal onto trigonometric signals and means for converting the modulated signal to an analog signal.

Cova teaches modulator for modulating the interpolated signal onto a trigonometric signal at a carrier frequency (see fig.4 element 411 and col.7, lines 18-20).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Cova into Blazo as to ensure that the modulation, up-conversion, down-conversion and demodulation would be accurately synchronized as taught by Cova (see col.7, lines 30-32)

As per claim 11, Cova teaches a digital to analog converter for converting the modulated signal to an analog signal (see fig.4 element 412). Furthermore implementing such teaching into Blazo would have been obvious to one skilled in the art as to produce an intermediate frequency output signal as taught by Cova (see col.6, lines 1-3).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wilson et al U.S. patent No 5,963,160 teaches an analog to digital conversion.

Donneley et al U.S. patent No 6,539,072 B1 teaches a delay locked loop.

Kakuishi et al U.S. Patent NO 5,615,235 teaches a signal processing system.

Leung et al U.S. patent No 5,485,490 teaches a method and circuitry for clock synchronization.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

9/11/04

EMMANUEL BAYARD
PRIMARY EXAMINER